

WHAT IS CLAIMED IS:

1. A circuit designing method comprising:

(a) separating a first algorithm description for a simulation into a hardware portion describing hardware and a software portion describing software, and generating a design data automatically, wherein said design data includes behavior data, architecture data, mapping data and address data;

(b) generating a first clock base description automatically based on said design data, wherein said first clock base description describes relation between said hardware portion and said software portion;

(c) generating a second clock base description automatically based on said design data, wherein said second clock base description describes said hardware portion; and

(d) generating a first CPU model automatically based on said design data, wherein said first CPU model describes said software portion,

wherein said first clock base description, said second clock base description and said first CPU model are used for verifying the design data.

2. The circuit designing method according to Claim 1, wherein said step (b) includes:

(b1) generating an address decoder portion automatically in said first clock base description based on said address data,

wherein said address decoder portion describes an address decoder which is arranged between a bus and a CUP interface in said first clock base description and selects an algorithm block from a plurality of algorithm blocks.

3. The circuit designing method according to Claim 2, wherein said step (b1) includes:

(b11) generating a bus connection between said bus and sad address decoder which is described by using a virtual bus in said first clock base description.

4. The circuit designing method according to Claim 1, wherein said step (a) includes:

(a1) converting said first algorithm description into second algorithm description automatically,

wherein it is easier for said second algorithm description to be separated into said hardware portion and said software portion than for said first algorithm description.

5. The circuit designing method according to Claim 4, wherein said step (a1) includes:

(a11) detecting first algorithm blocks from a plurality of algorithm blocks included in said first algorithm description, wherein data flow in one way between said first algorithm blocks through a global variable; and

(a12) replacing said global variable associated to said first algorithm blocks to a port.

6. The circuit designing method according to Claim 3, wherein said step (a) includes:

(a2) converting said first algorithm description into second algorithm description automatically,

wherein it is easier for said second algorithm description to be separated into said hardware portion and said software portion than for said first algorithm description.

7. The circuit designing method according to Claim 6, wherein said step (a2) includes:

(a21) detecting first algorithm blocks from a plurality of algorithm blocks included in said first algorithm description, wherein data flow in one way between said first algorithm blocks through a global variable; and

(a22) replacing said global variable associated to said first algorithm blocks to a port.

8. The circuit designing method according to Claim 1, further comprising:

(e) generating a first HDL description automatically based on said design data, wherein said first HDL description indicates relation between said hardware portion and said software portion;

(f) generating a second HDL description automatically based on said design data, wherein said second HDL description indicates said hardware portion; and

(g) generating a second CPU model automatically based on said design data, wherein said second CPU model indicates said software portion,

wherein said first HDL description, said second HDL description and said second CPU model are used for verifying the design data.

9. A circuit designing method comprising:

(h) separating a first algorithm description for a simulation into a hardware portion describing hardware and a software portion describing software, and generating a design data automatically, wherein said design data includes behavior data, architecture data, mapping data and address data;

(i) generating a first clock base description automatically based on said design data, wherein said first clock base description describes relation between said hardware portion and said software portion;

(j) generating a second clock base description automatically based on said design data, wherein said second clock base description describes said hardware portion;

(k) generating a first CPU model automatically based on said design data, wherein said first CPU model describes said software portion; and

(l) carrying out said simulation to verify the design data by using said first clock base description, said second clock base description and said first CPU model.

10. The circuit designing method according to Claim 9, further comprising:

- (m) generating a first HDL description automatically based on said design data, wherein said first HDL description indicates relation between said hardware portion and said software portion;
- (n) generating a second HDL description automatically based on said design data, wherein said second HDL description indicates said hardware portion;
- (o) generating a second CPU model automatically based on said design data, wherein said second CPU model indicates said software portion; and
- (p) carrying out said simulation to verify the design data by using said first HDL description, said second HDL description and said second CPU model.

11. A circuit designing system comprising:

- an algorithm design apparatus which separates a first algorithm description for a simulation into a hardware portion describing hardware and a software portion describing software, and generates a design data automatically, wherein said design data includes behavior data, architecture data, mapping data and address data;
- a first clock base description generating apparatus which generates a first clock base description automatically based on said design data, wherein said first clock base description describes relation between said hardware portion and said software portion;
- a second clock base description generating apparatus which generates a second clock base description automatically based on said design data, wherein said second clock base description describes said hardware portion; and
- a first CPU model generating apparatus which generates a first CPU model automatically based on said design data, wherein said first CPU model describes said software portion,

wherein said first clock base description, said second clock base description and said first CPU model are used for verifying the design data.

12. The circuit designing system according to Claim 11, wherein said first clock base description generating apparatus generates an address decoder portion automatically in said first clock base description based on said address data,

wherein said address decoder portion indicates an address decoder which is arranged between a bus and a CUP interface in said first clock base description and selects an algorithm block from a plurality of algorithm blocks.

13. The circuit designing system according to Claim 12, wherein said first clock base description generating apparatus generates a bus connection between said bus and said address decoder which is described by using a virtual bus in said first clock base description.

14. The circuit designing system according to Claim 11, wherein said algorithm design apparatus converts said first algorithm description into second algorithm description automatically,

wherein it is easier for said second algorithm description to be separated into said hardware portion and said software portion than for said first algorithm description.

15. The circuit designing system according to Claim 14, wherein said algorithm design apparatus detects first algorithm blocks from a plurality of algorithm blocks included in said first algorithm description, wherein data flow in one way between said first algorithm blocks through a global variable, and replaces said global variable associated to said first algorithm blocks to a port.

16. The circuit designing system according to Claim 13, wherein said algorithm design apparatus converts said first algorithm description into second algorithm description automatically,

wherein it is easier for said second algorithm description to be separated into said hardware portion and said software portion than for said first algorithm description.

17. The circuit designing system according to Claim 16, wherein said algorithm design apparatus detects first algorithm blocks from a plurality of algorithm blocks included in said first algorithm description, wherein data flow in one way between said first algorithm blocks through a global variable, and replaces said global variable associated to said first algorithm blocks to a port.

18. The circuit designing system according to Claim 1, further comprising:

a first HDL description generating apparatus which generates a first HDL description automatically based on said design data, wherein said first HDL description indicates relation between said hardware portion and said software portion;

a second HDL description generating apparatus which generates a second HDL description automatically based on said design data, wherein said second HDL description indicates said hardware portion; and

a second CPU model generating apparatus which generates a second CPU model automatically based on said design data, wherein said second CPU model indicates said software portion,

wherein said first HDL description, said second HDL description and said second CPU model are used for verifying the design data.

19. A circuit designing system comprising::

an algorithm design apparatus which separates a first algorithm description for a simulation into a hardware portion describing hardware and a software portion describing software, and generates a design data automatically, wherein said design data includes behavior data, architecture data, mapping data and address data;

- a first clock base description generating apparatus which generates a first clock base description automatically based on said design data, wherein said first clock base description describes relation between said hardware portion and said software portion;

a second clock base description generating apparatus which generates a second clock base description automatically based on said design data, wherein said second clock base description describes said hardware portion;

a first CPU model generating apparatus which generates a first CPU model automatically based on said design data, wherein said first CPU model describes said software portion; and

a clock base simulation executing apparatus which carries out said simulation to verify the design data by using said first clock base description, said second clock base description and said first CPU model.

20. The circuit designing system according to Claim 19, further comprising:

a first HDL description generating apparatus which generates a first HDL description automatically based on said design data, wherein said first HDL description indicates relation between said hardware portion and said software portion;

a second HDL description generating apparatus which generates a second HDL description automatically based on said design data, wherein said second HDL description indicates said hardware portion;

a second CPU model generating apparatus which generates a second CPU model automatically based on said design data, wherein said second CPU model indicates said software portion; and

a HDL simulation executing apparatus which carries out said simulation to verify the design data by using said first HDL description, said second HDL description and said second CPU model.

21. A computer program product embodied on a computer-readable medium and comprising code that, when executed, causes a computer to perform the following:

(a) separating a first algorithm description for a simulation into a hardware portion describing hardware and a software portion describing software, and generating a design data automatically, wherein said design data includes behavior data, architecture data, mapping data and address data;

(b) generating a first clock base description automatically based on said design data, wherein said first clock base description describes relation between said hardware portion and said software portion;

(c) generating a second clock base description automatically based on said design data, wherein said second clock base description describes said hardware portion; and

(d) generating a first CPU model automatically based on said design data, wherein said first CPU model describes said software portion,

wherein said first clock base description, said second clock base description and said first CPU model are used for verifying the design data.

22. The computer program product according to Claim 21, wherein said step (b) includes:

(b1) generating an address decoder portion automatically in said first clock base description based on said address data,

wherein said address decoder portion indicates an address decoder which is arranged between a bus and a CUP interface in said first clock base description and selects an algorithm block from a plurality of algorithm blocks.

23. The computer program product according to Claim 22, wherein said step (b1) includes:

- (b11) generating a bus connection between said bus and sad address decoder which is described by using a virtual bus in said first clock base description.

24. The computer program product according to Claim 21, wherein said step (a) includes:

(a1) converting said first algorithm description into second algorithm description automatically,

wherein it is easier for said second algorithm description to be separated into said hardware portion and said software portion than for said first algorithm description.

25. The computer program product according to Claim 24, wherein said step (a1) includes:

(a11) detecting first algorithm blocks from a plurality of algorithm blocks included in said first algorithm description, wherein data flow in one way between said first algorithm blocks through a global variable; and

(a12) replacing said global variable associated to said first algorithm blocks to a port.

26. The computer program product according to Claim 23, wherein said step (a) includes:

(a2) converting said first algorithm description into second algorithm description automatically,

wherein it is easier for said second algorithm description to be separated into said hardware portion and said software portion than for said first algorithm description.

27. The computer program product according to Claim 26, wherein said step (a2) includes:

(a21) detecting first algorithm blocks from a plurality of algorithm blocks included in said first algorithm description, wherein data flow in one way between said first algorithm blocks through a global variable; and

- (a22) replacing said global variable associated to said first algorithm blocks to a port.

28. The computer program product according to Claim 21, further comprising:

(e) generating a first HDL description automatically based on said design data, wherein said first HDL description indicates relation between said hardware portion and said software portion;

(f) generating a second HDL description automatically based on said design data, wherein said second HDL description indicates said hardware portion; and

(g) generating a second CPU model automatically based on said design data, wherein said second CPU model indicates said software portion,

wherein said first HDL description, said second HDL description and said second CPU model are used for verifying the design data.

29. A computer program product embodied on a computer-readable medium and comprising code that, when executed, causes a computer to perform the following:

(h) separating a first algorithm description for a simulation into a hardware portion describing hardware and a software portion describing software, and generating a design data automatically, wherein said design data includes behavior data, architecture data, mapping data and address data;

(i) generating a first clock base description automatically based on said design data, wherein said first clock base description describes relation between said hardware portion and said software portion;

(j) generating a second clock base description automatically based on said design data, wherein said second clock base description describes said hardware portion;

(k) generating a first CPU model automatically based on said design data, wherein said first CPU model describes said software portion; and

(l) carrying out said simulation to verify the design data by using said first clock base description, said second clock base description and said first CPU model.

30. The computer program product according to Claim 29, further comprising:

(m) generating a first HDL description automatically based on said design data, wherein said first HDL description indicates relation between said hardware portion and said software portion;

(n) generating a second HDL description automatically based on said design data, wherein said second HDL description indicates said hardware portion;

(o) generating a second CPU model automatically based on said design data, wherein said second CPU model indicates said software portion; and

(p) carrying out said simulation to verify the design data by using said first HDL description, said second HDL description and said second CPU model.